High-voltage-compatible, fully depleted CCDs

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ABSTRACT

We describe charge-coupled device (CCD) development activities at the Lawrence Berkeley National Laboratory (LBNL). Back-illuminated CCDs fabricated on 200–300 μm thick, fully depleted, high-resistivity silicon substrates are produced in partnership with a commercial CCD foundry. The CCDs are fully depleted by the application of a substrate bias voltage. Spatial resolution considerations require operation of thick, fully depleted CCDs at high substrate bias voltages. We have developed CCDs that are compatible with substrate bias voltages of at least 200V. This improves spatial resolution for a given thickness, and allows for full depletion of thicker CCDs than previously considered. We have demonstrated full depletion of 650–675 μm thick CCDs, with potential applications in direct x-ray detection. In this work we discuss the issues related to high-voltage operation of fully depleted CCDs, as well as experimental results on high-voltage-compatible CCDs.

Keywords: CCD, PSF, fully depleted, high voltage, channel stop, static induction transistor, x-ray detection

1. INTRODUCTION

Mosaics of back-illuminated, fully depleted silicon imagers are of increasing interest for scientific applications. For example, fully depleted imagers are planned for the proposed Large Synoptic Survey Telescope (LSST),[1] the Dark Energy Survey camera,[2] the Subaru Telescope HyperSuprime camera upgrade,[3] and the SuperNova Acceleration Probe (SNAP),[4] a proposed space-based dark energy mission.

The increased interest in fully depleted silicon imagers arises from the advantages these devices have over conventional, thinned CCDs that are typically 10–20 μm thick. The ability to make thick imagers results in improved quantum efficiency (QE) at near-infrared (NIR) wavelengths when compared to conventional back-illuminated CCDs. In addition, fringing due to multiply reflected light is greatly reduced. By combining high-resistivity, n-type silicon substrates with a substrate bias voltage, we have developed fully depleted, back-illuminated CCDs that are 200–300 μm thick,[5–8] and have reported imaging and spectroscopy results for astronomical applications at wavelengths up to approximately 1 μm.[6, 8] In addition, recently a fully depleted CCD developed at a commercial company was described,[3] and hybrid imagers with CMOS readout circuitry bump bonded to fully depleted pin diode arrays are available commercially from two suppliers.[9, 10]

A potential advantage of thick imagers is a simplified fabrication process. Thinning of CCDs to 10–20 μm thickness is not amenable to batch fabrication techniques, and this along with limited demand results in a high cost for conventional scientific CCDs. We have described fabrication techniques that allow for the steps necessary to produce back-illuminated CCDs to be performed at the wafer level.[6, 7] In particular, we have demonstrated that lithography, etch and thin-film deposition steps can be performed on 150 mm diameter silicon wafers that are 200 μm thick.[7] This allows for the simultaneous fabrication of multiple devices, which is more in line with conventional fabrication of mainstream integrated circuits.

Fully depleted CCDs and hybrid CMOS imagers also have a point spread function (PSF) that can be controlled by adjusting the substrate thickness and the substrate bias voltage. This is in contrast to conventional thinned CCDs where diffusion in the field-free region at the backside of the CCD usually dominates the PSF.[6] As described in the following section, the ability to improve the PSF by operating at high substrate bias voltages is a major motivation for the effort described in this work.

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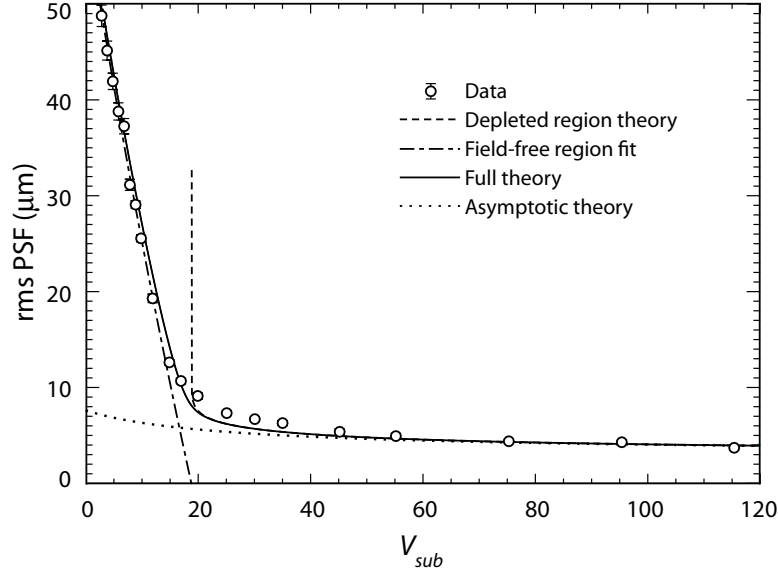S.E.H.: E-mail: seholland@lbl.gov, Telephone: 1 510 486 5069

Figure 1. Measured rms diffusion (PSF) for a CCD of the type described in this work.[11]   The CCD used for this measurement was 3512^2 with 10.5 μm pixels, and was approximately 200 μm thick.

2. MOTIVATION FOR HIGH-VOLTAGE-COMPATIBLE CCD DEVELOPMENT

For the LSST and SNAP applications mentioned above, spatial resolution is an important consideration. For a thick, back-illuminated CCD the photogenerated charge will diffuse laterally during the transit to the CCD potential wells. Minimizing the transit time is key to achieving a good PSF. It has been shown that fully depleted CCDs have a PSF that is linearly dependent on the CCD thickness, and inversely proportional to the square root of the substrate bias voltage that is used to overdeplete the CCD.[6] For high NIR QE one desires a thick detector, but this degrades the PSF. If operation at high substrate bias voltages were possible, however, the tradeoffs in QE and PSF would not be as severe as those resulting when only relatively low voltage substrate bias voltages are practical.

Figure 1 shows measured rms PSF due to lateral diffusion of photogenerated charge for a CCD of the type described in this report. The curve labeled "asymptotic theory" includes the electric field dependence of hole mobility, which is necessary in order to accurately fit the data.[11]   As an example, the SNAP requirement for a weak-lensing survey is a PSF of 4 μm, and it can be seen that a substrate bias voltage in the 100V range is required to achieve this for the approximately 200 μm thick CCD used for the measurements shown in Fig. 1.

As a result of these considerations, we have developed fully depleted CCDs that can be operated at substrate bias voltages of at least 200V, thereby allowing for simultaneous high QE in the NIR and good PSF. In the next section we describe some of the issues related to operation of fully depleted CCDs at high substrate bias voltages, followed by experimental results on prototype CCDs for SNAP.

3. HIGH-VOLTAGE CONSIDERATIONS

Several deleterious effects can occur when CCDs are operated at high voltages. The gate insulator in the imaging area can be catastrophically damaged if the dielectric breaks down due to an overvoltage condition. Scientific CCDs have gate insulator breakdown voltages in the 80–100V range, and therefore operation at substrate bias voltages exceeding that is cause for concern. Short of permanent failure, overvoltages on the gate dielectric can cause threshold voltage shifts resulting in a cumulative degradation of the CCD properties over time. In addition, high electric fields at the silicon surface of the CCD can result in avalanche breakdown in the silicon, the effects of which can range from excess noise to complete failure of the device.
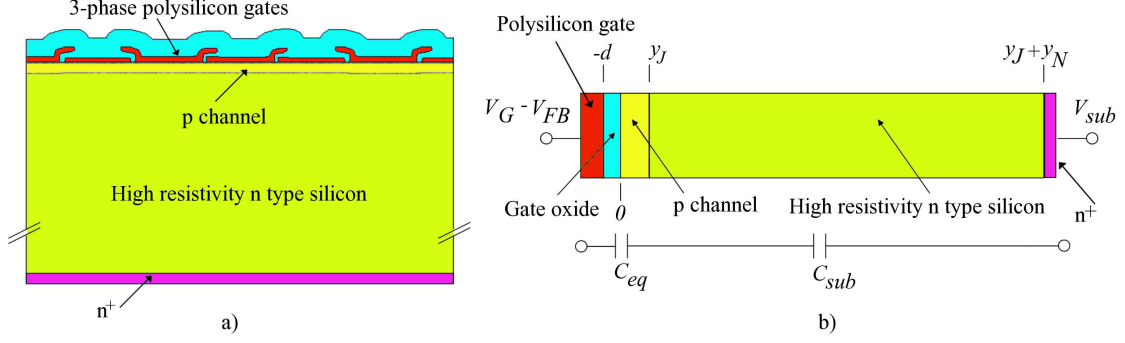
Figure 2. a) Cross-sectional diagram of the CCD described in this work. The CCD is fully depleted by the application of a substrate bias voltage. b) Simplified cross section used in the solution of the 1D Poisson equation and the equivalent circuit.

In order to develop fully depleted CCDs that can function at high substrate bias voltages, one must have a detailed knowledge of the internal potentials and electric fields in the CCD and how they are affected by the substrate bias voltage. We have relied on both 1 dimensional (1D) analytic calculations and 2 dimensional (2D) simulations to better understand the issues that arise when one attempts to bias fully depleted CCDs at high voltages.

3.1. Channel potential considerations

Figure 2 a) shows a simplified cross-sectional diagram of the type of CCD considered in this work, representing a 3-phase, buried-channel CCD fabricated on a high-resistivity, n-type substrate that is fully depleted by the bias voltage applied at the backside of the device. The backside n^+ layer is necessary for low dark current. The heavily doped region passivates the interface states at the backside silicon surface and prevents the depletion region from extending to that surface. As shown later this is especially critical when the CCD is operated overdepleted. In the actual implementation the bias voltage is applied to the front side of the CCD to allow for the use of insulating anti-reflecting coatings and to simplify the packaging.[6]

It was shown previously from a 1D solution of the Poisson equation along the y direction of Fig. 2 that the potential minimum in the buried channel is approximately equal to the potential V_J at the buried channel-substrate junction, which in turn is approximately

$$V_J \approx V_G - V_{FB} - \frac{q\,N_A}{2\,\epsilon_{\mathrm{Si}}}\,y_J{}^2 \left(1 + \frac{2\,\epsilon_{\mathrm{Si}}\,d}{\epsilon_{\mathrm{SiO_2}}\,y_J}\right). \tag{1}$$

V_G is the applied gate voltage, V_{FB} is the flat-band voltage, q is the electron charge, N_A is the doping density in the p-channel, y_J is the buried-channel thickness, d is the gate insulator thickness, and ϵ_{Si} and $\epsilon_{\mathrm{SiO_2}}$ are the permittivities of silicon and silicon dioxide, respectively. To simplify the 1D calculations the doping profiles are taken to be constant.

Equation (1) implies that V_J is independent of V_{sub}, the substrate bias voltage. Figure 2 b) shows the simplified cross section used for the 1D calculation along with an equivalent circuit assuming the buried channel and high-resistivity, n-type substrate are fully depleted. The equivalent circuit can be represented by a capacitor voltage divider where C_{sub} is $\epsilon_{\mathrm{Si}}/y_N$ and C_{eq} is the series combination of the buried-channel capacitance $C_{bc} = \epsilon_{\mathrm{Si}}/y_J$ and the gate insulator capacitance $C_{\mathrm{ins}} = \epsilon_{\mathrm{SiO_2}}/d$. y_N is the thickness of the fully depleted n-type substrate. For thick substrates, $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})\,d$ and the channel potential is a weak function of the substrate bias as a result of C_{sub} being much smaller than the series combination of C_{bc} and C_{ins}.[6]

As a result of these considerations we conclude that the channel potential is not a limiting factor in terms of high voltages applied to the substrate. The channel potential is approximately independent of the substrate bias voltage when the high-resistivity substrate is thick and fully depleted. Of more concern are the channel-stop regions in the CCD imaging area and elsewhere. This is discussed in the following section.
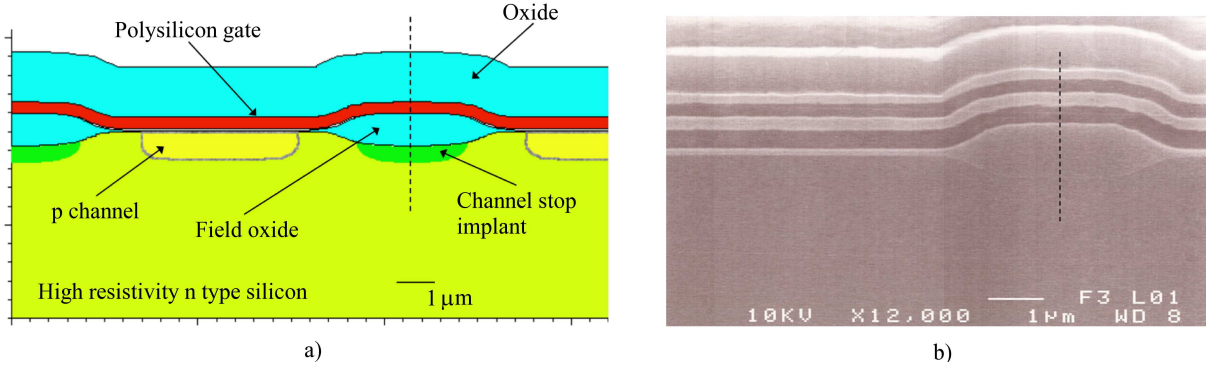
Figure 3. a) Cross-sectional drawing of the channel and channel stop region. This view is orthogonal to that shown in Fig. 2 a). b) Scanning electron microscope picture showing the cross section of a channel and channel-stop region (courtesy Robert Groulx, DALSA Semiconductor). The dashed line in both figures bisects the channel-stop region.
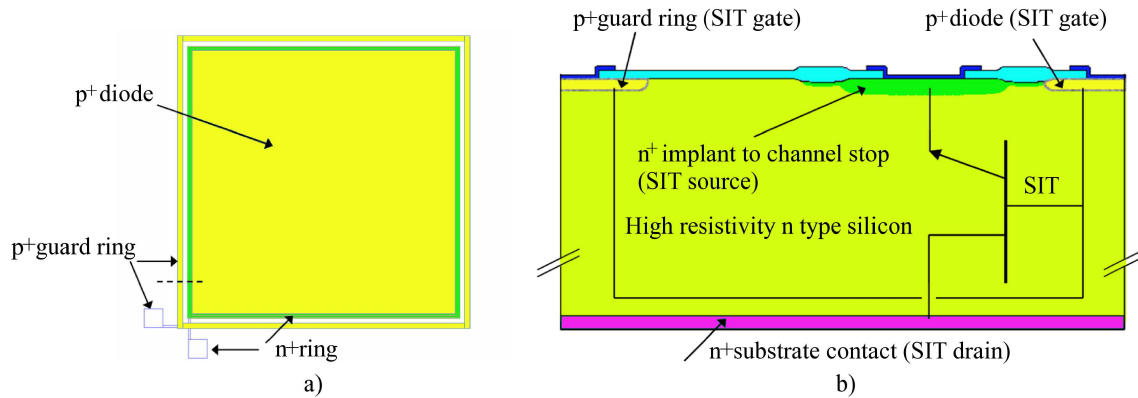

Figure 4. a) Plan view of a p-i-n diode test structure used to measure dark current. b) Cross-sectional view taken along the dashed line of a), and showing a parasitic static induction transistor.

3.2. Channel-stop potentials

The channel stop consists a thick field oxide grown over an implanted region. Channel stops are present in all areas that do not contain active elements such as CCD channels and transistors. Figure 3 a) shows a cross-sectional drawing of the CCD channel and channel-stop regions in the imaging area. The cross section shown in Fig. 3 a) is orthogonal to that shown in Fig. 2 a). Figure 3 b) shows a scanning electron microscope picture of the CCD channel and channel-stop regions. In the imaging area the channel stop prohibits photogenerated charge from spilling over to adjacent columns.

In conventional scientific CCDs the channel-stop region is typically electrically grounded, as is the substrate. This allows for the reduction of surface dark current due to silicon-silicon dioxide interface states in the buried-channel region. By clocking the CCD gate electrodes in such a way as to invert the surface with carriers supplied from the channel stops, one can achieve a significant reduction in surface dark current.[12]

The use of large substrate bias voltages is incompatible with the grounding of the channel stops. At sufficiently high substrate bias voltages a punch-through current can flow between the grounded channel stops and the backside substrate contact. This is analogous to a static induction transistor (SIT).[13] A CCD with a nonzero substrate bias voltage has parasitic SITs that must be taken into account. As an example of a parasitic SIT, Fig. 4 a) shows a p-i-n diode test structure that was included on early LBNL CCD designs. This test structure was used to measure the dark current, which is a sensitive indicator of the quality of the fabrication process. As shown below it can also be biased as a SIT.
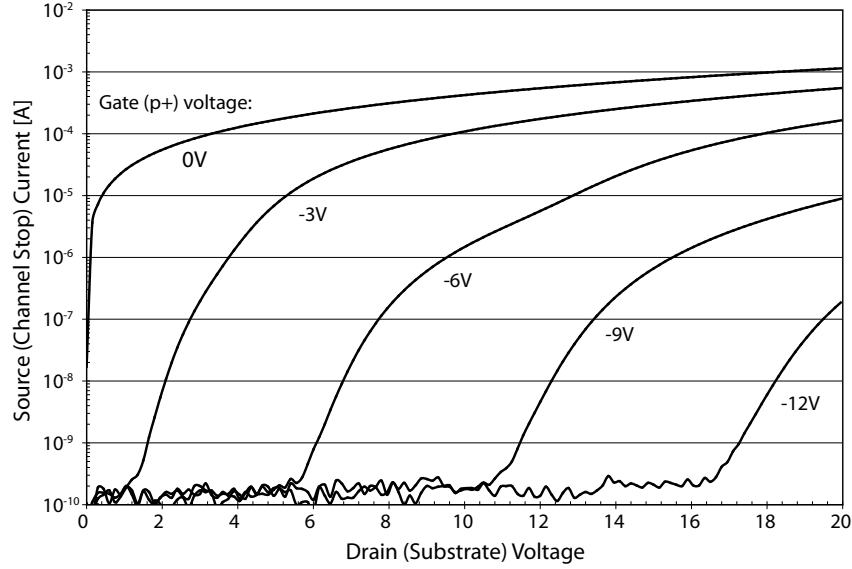
Figure 5. Measured current-voltage characteristics of the p-i-n diode structure of Fig. 4 when biased as a parasitic static induction transistor. The p^+ regions are the SIT gates, the n^+ contact to the channel stop functions as the SIT source, and the backside n^+ contact is the SIT drain. The source is grounded during the measurement.

In normal operation the p^+ diode and guard rings are grounded, and the p^+ diode dark current is measured as the substrate bias voltage is varied. The function of the p^+ guard ring is to collect dark current generated beyond the periphery of the p^+ diode. In the more recent LBNL designs multiple guard ring structures are used for improved high-voltage performance.[6]

Also included in this particular test structure was an n^+ ring between the p^+ guard ring and diode. Figure 4 b) shows a cross-sectional drawing through a line that includes from left to right the p^+ guard ring, the n^+ ring, and the p^+ diode. The n^+ ring connection to the channel stop allows this test structure to function as a SIT. The channel stops are the SIT sources, and the SIT gates are the p^+ regions on both sides of the channel stop in Fig. 4 a). The SIT drain is the backside n^+ contact where the substrate bias voltage is applied.

Figure 5 shows the measured current-voltage characteristics when the p-i-n diode of Fig. 4 is operated as a SIT, where the source (channel stop) current is measured as a function of the drain (substrate) voltage with the gate (p^+) to source voltage as a parameter. The reverse bias between gate and source pinches off the vertical conduction path, but as seen in Fig. 5 it becomes increasingly more difficult to suppress the SIT current as the drain (substrate) voltage is increased. Also, the parasitic SIT currents are quite large for this case of a p^+ diode area of 2 mm^2 with a 50 μm gap between the p^+ regions, even at 20V substrate bias. This electron current is sinked at the substrate bias voltage source, and the power dissipation would be significant if such large currents were allowed to flow in fully depleted CCDs biased at large substrate voltages.

The use of grounded channel stops in the CCD imaging array in conjunction with the application of a substrate bias voltage has been reported.[14] In the n-channel CCD described, n^+ guard rings were reverse biased with respect to the p-type channel stops to suppress the SIT current. However, a punch-through current of approximately 10 μA was reported at a substrate bias of -40V for a relatively small CCD (512^2). This current was believed to arise from regions outside of the imaging array and therefore would be expected to scale with CCD size.

As discussed earlier, PSF requirements for SNAP have resulted in a need to operate at substrate bias voltages of approximately 100V. As a result of this high-voltage requirement, we have taken a different approach to the channel-stop problem. We have attempted to engineer the channel stops to minimize the resulting surface potentials and electric fields, and bias the channel stops in such a way as to prohibit conduction of the parasitic SITs.

In the imaging area the channel stops are covered by polysilicon gates (Fig. 3), and we have investigated and implemented fully depleted channel stops. The full depletion of the channel stop results from the field effect due to the biased polysilicon gate over the field oxide. The effect of the substrate voltage is to add to the total voltage across the MOS capacitor formed by the polysilicon gate, the field oxide, the channel-stop implant, and the high-resistivity substrate. A concern is the maximum potential that results when the channel stop is fully depleted at high substrate bias voltages. A 1D solution to the Poisson equation for the channel-stop region yields a surface potential that is given by

$$V_{\text{surface}} = V_G - V_{FB} + A\, d_{cs} \tag{2}$$

where V_{surface} is the potential in the channel stop at the silicon-silicon dioxide interface and d_{cs} is the field-oxide thickness. A is

$$A = \frac{V_{\text{sub}} - (V_G - V_{FB}) + (q\, N_{D,cs}/\epsilon_{\text{Si}})\left(y_{cs}{}^2/2 + y_{cs}\, y_N\right) + \left(q\, N_{D,\text{sub}}\, y_N{}^2\right)/\left(2\, \epsilon_{\text{Si}}\right)}{(\epsilon_{\text{SiO}_2}/\epsilon_{\text{Si}})\,(y_N + y_{cs}) + d_{cs}} \tag{3}$$

where $N_{D,cs}$ is the doping level of the channel-stop implant, $N_{D,\text{sub}}$ is the doping level in the n-type substrate, and y_{cs} and d_{cs} are the thicknesses of the channel-stop implant and field oxide, respectively. The cross section for this calculation is similar to that shown in Fig. 2 b), with the p-channel region replaced with an n-type, channel-stop region. An assumption used in the derivation of Eq. (2) is that the surface does not invert with holes, which is valid in the imaging array due to the nearby p channels that are at a lower potential than the channel stop and which will collect holes.

For a thick, fully depleted substrate with $y_{cs} \ll y_N$ and $N_{D,cs} \gg N_{D,\text{sub}}$ the surface potential is approximately given by

$$V_{\text{surface}} \approx V_G - V_{FB} + \frac{q\, N_{D,cs}\, y_{cs}}{C_{ox,cs}}, \tag{4}$$

which is independent of V_{sub} as was the case in Eq. (1). The field-oxide capacitance per unit area $C_{ox,cs}$ is $\epsilon_{\text{SiO}_2}/d_{cs}$. The channel-stop potential at the surface is proportional to the field-oxide thickness and channel-stop doping, as seen in the third term of Eq. (4), which is the voltage drop across the field oxide. The calculated surface potential from the 1D model for a 1 μm field-oxide thickness and channel-stop doping density of 1×10^{16} cm^{-3} is approximately 53V, assuming $V_G - V_{FB}$ is 6V and y_{cs} is 1 μm. Such a high potential in proximity to the CCD channels raises concerns about the possibility of excessively high electric fields in the CCD imaging area. However, if the field-oxide thickness is reduced to 0.25 μm the calculated surface potential is approximately 18V. Therefore, for high-voltage-compatible CCDs, there is benefit in engineering the channel stop to reduce surface potentials. Note that the flatband voltage contains a term due to fixed oxide charge, i.e. $Q_F/C_{ox,cs}$, and the effect of fixed oxide charge for an n-type channel stop is to increase the surface potential since Q_F is always a positive charge. Field oxides generally have relatively high Q_F and the flatband voltage term is typically non-negligible.

In collaboration with DALSA Semiconductor we have fabricated high-voltage-compatible CCDs with varying field-oxide thicknesses of $\approx$ 0.8 μm, 0.5 μm, and 0.25 μm. We have measured channel-stop potentials using a high-impedance electrometer and the results are shown in Fig. 6. For these CCDs an n$^+$ implant runs perpendicular to the CCD columns and splits the imaging array into two halves. This results in a dead space 2 rows wide in the center of the CCD where one can measure the channel-stop potentials. As seen in Fig. 6 the channel-stop potentials tend to saturate at sufficiently high substrate bias, and the saturation value scales with field-oxide thickness as predicted by Eqs. (2) and (4). The saturation value is also independent of CCD thickness, as expected. The results shown in Fig. 6 are in qualitative agreement with 2D simulations of the vertical clock bus region, which consists of a fairly wide region ($\approx$ 80 μm) where the channel stops are fully depleted and where the 1D calculations are expected to apply. Figure 6 demonstrates the usefulness of fully depleting the channel stop and using reduced thickness field oxides in order to reduce surface potentials when high substrate bias voltages are used.
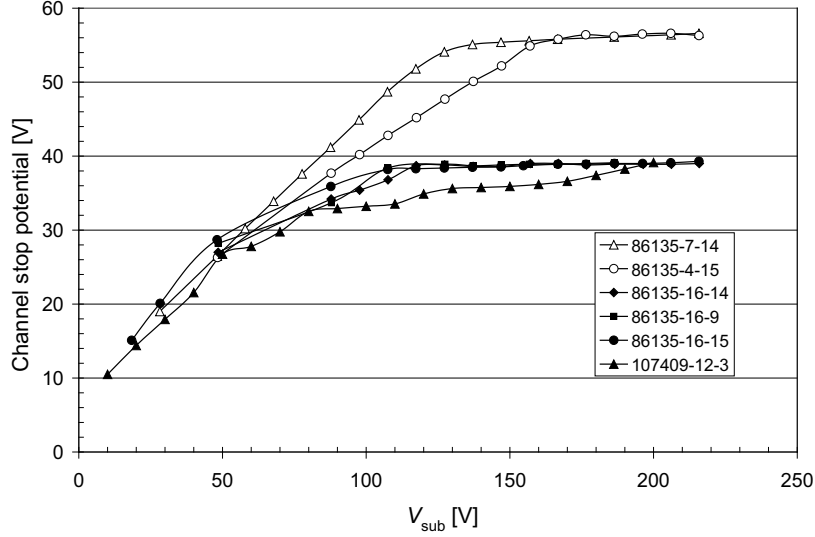
Figure 6. Measured channel-stop potentials. The open and closed symbols correspond to field-oxide thicknesses of $\approx 0.8~\mu$m and 0.5 μm, respectively. The device code is lot number-wafer number-device number. All 86135 devices are 3512^2, 10.5 μm CCDs while 107409-12-3 is a 1700×1836, 10.5 μm CCD. 107409-12-3 is 200 μm thick, 86135-7-14 is 250 μm thick, and the remaining CCDs are $\approx 650~\mu$m thick.

The channel stops in the CCD imaging area are narrow, *e.g.* 3 μm in the present CCD designs. The adjacent channel potentials are approximately -9V at the potential minimum for the collecting phases according to 2D simulations. This fairly large negative potential in proximity to the relatively large positive potential in the fully depleted channel stop is expected to result in significant 2D effects in terms of the potentials in the imaging array. Figure 7 shows the results of 2D simulations of the channel and channel-stop potentials. Simulation cross sections similar to that shown in Fig. 3 a) were generated with the process simulation program TSUPREM4.[15] The field-oxidation cycles were adjusted in the simulations to yield field-oxide thicknesses comparable to the actual ones achieved in the processing at DALSA Semiconductor. The resulting simulated field-oxide thicknesses were 0.866, 0.540, and 0.265 μm. The simulation cross sections were then exported to the 2D device simulator Medici[15] for calculations of the electrostatic potentials.

The surface potentials shown in Fig. 7 are calculated along a horizontal line in Fig. 3 a) at a depth corresponding to the interface between the silicon and the field oxide where the channel-stop potential is maximized. Since silicon is consumed during oxidation, the depths vary for the different field-oxide thicknesses. The peaks in the potential correspond to the center of the 3 μm wide channel stops, and the minimums are at the centers of the buried channels. The polysilicon gate voltage was 5V to simulate the barrier phase. The substrate bias voltage used in the simulation was 200V.

The trend of higher channel-stop potential with thicker field oxide is evident in Fig. 7. However, as a result of the strong 2D effects the potentials are lower than predicted from the 1D analytic model (Eqs. (2) and (4)), especially for the thickest field oxide where the vertical field coupling between the polysilicon gate and channel stop is the weakest. Nonetheless, it is clear from Figs. 6 and 7 that by proper channel-stop engineering one can reduce surface potentials with fully depleted channel stops via the field effect when the channel stops are covered by polysilicon gates.

A drawback to fully depleting the channel stops in this manner is the inability to take advantage of surface inversion to reduce dark current. At the operating temperature for SNAP (≈ -140 ºC), however, the surface dark current can be reduced by inverting the buried-channel surface between frames at 0V substrate bias and taking advantage of the long time constants at low temperatures for charge trapped at interface states.[6, 16]

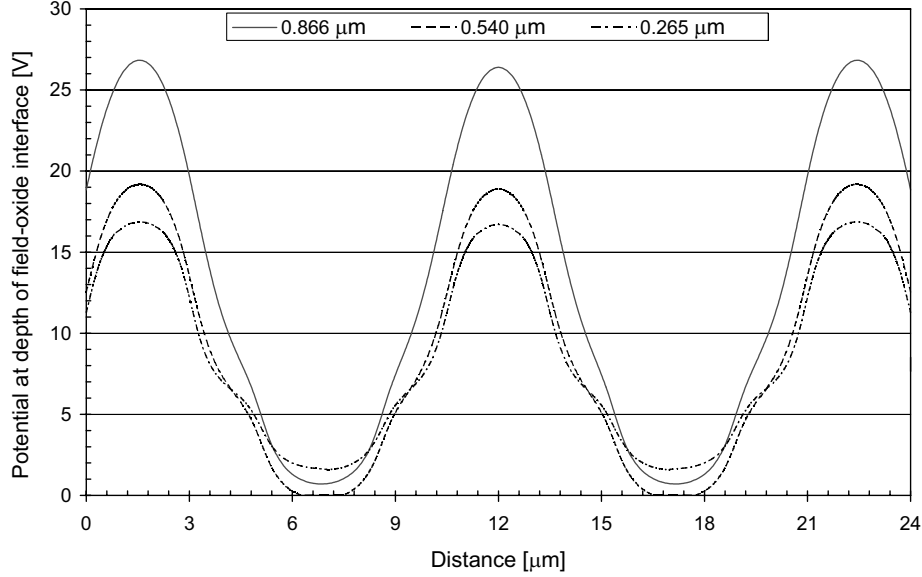In other areas of the CCD, for example near the output transistors, it is not always practical to fully deplete

Figure 7. Simulated channel and channel-stop potentials for field-oxide thicknesses of 0.866, 0.540, and 0.265 μm. The potential is calculated at a depth along a horizontal line corresponding to the interface between the silicon and the field oxide, which varies due to silicon consumption during oxidation (see Fig. 3). The peaks correspond to the center of the channel-stop region, and the valleys are at the centers of the buried channels.

the channel stops with the field effect. The channel-stop potentials arising in this case, *i.e.* without the field effect due to gate electrodes, are similar to potentials in p-i-n strip detectors used in high-energy-physics experiments that require inversion-blocking implants.[17] In the high-energy-physics detectors the magnitude of the floating potential of the implanted region (analagous to the channel stop) between junctions increases with increasing junction spacing (SIT gate to gate spacing, *e.g.* Fig. 4b). The floating potential is a measure of the potential at the SIT source that is necessary to drain the leakage current generated in the source region of the parasitic SIT, and corresponds to the threshold of conduction. We have observed that this potential increases approximately linearly with substrate bias voltage with a slope and magnitude dependent on geometry and fixed oxide charge density.

However, in contrast to strip detectors, the channel-stop region around the output transistors cannot be allowed to electrically float. Related to this, we have observed anomalous effects in CCDs that did not have low-impedance connections to the channel stops near the output transistor. These included drifting baselines and large zero-signal levels. The latter were believed to arise from double correlated sampling of slowly varying transients introduced by clock feedthroughs to the channel stop, which had a high impedance to the external connection point. In extreme cases it is possible to form electrically floating islands of channel stop around the output transistors due to metal and polysilicon electrodes fully depleting the channel stops beneath the electrodes. Our approach is to engineer the channel-stop regions to reduce the potentials near the output transistors, and to bias the channel stops to form a low-impedance ac ground while probibiting conduction of the parasitic SIT. The channel-stop connection consists of a metal contact to a high dose n^+ implant that abuts the channel-stop region (*e.g.* Fig. 4b).

Figure 8 shows measured channel-stop potentials versus substrate bias voltage for an experimental CCD with channel-stop connections near each of four output amplifiers as well as in the imaging region. As in Fig. 6 the potential in the imaging area is measured at a channel-stop connection consisting of an n^+ implant in the row direction that splits the imaging array in half. The spacing between the p^+ guard rings and the p and p^+ regions of the extended serial register and reset/output transistors was intentionally varied on each half of the CCD, *i.e.* varying the spacing between gates of the parasitic SITs (*e.g* Fig. 4). The n^+ implanted contacts to the channel stops were inserted between the guard rings and p and p^+ regions. As seen in Fig. 8 the measured potential is largest on the channel stops near the amplifiers on the bottom half of the CCD, which also corresponds to a larger
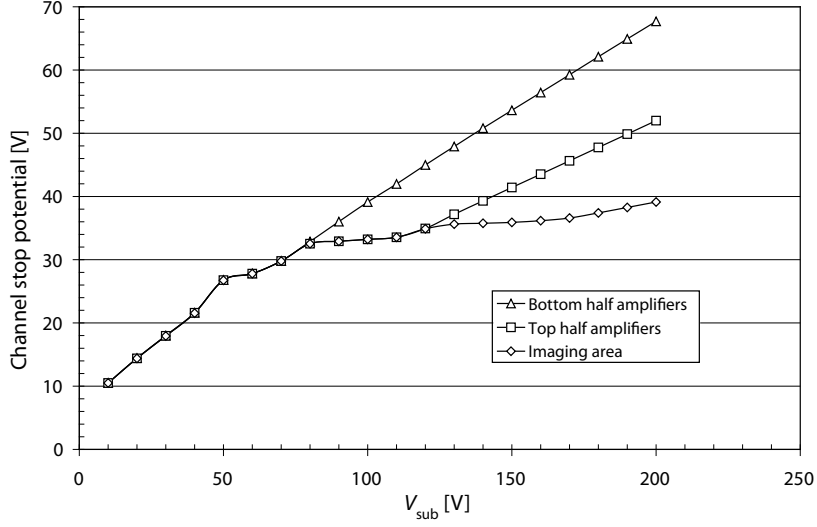
Figure 8. Measured channel-stop potentials for CCD 107409-12-3. This CCD has channel-stop connections near the 4 output amplifiers and in the imaging area via an n$^+$ implant that splits the imaging array in half. For a given half the potentials measured near the output amplifiers were essentially identical, so only one measurement for each half is shown for clarity.

parasitic SIT gate spacing when compared to the top half of the CCD. The lowest potential is measured in the imaging area, and as described earlier this potential is determined by full depletion of channel-stop regions under polysilicon gates. When all five channel-stop regions are connected together, the measured potential follows the highest potential of the five, consistent with the fact that the most difficult to turn off SIT dominates the measured potential.

The lowest potentials we have measured are for 3512^2, 10.5 μm pixel CCDs with a field-oxide thickness of ≈ 0.25 μm and a SIT gate-to-gate spacing corresponding to the "top side amplifiers" case of Fig. 8. At high substrate bias voltages the potential is dominated by the channel-stop potentials near the output amplifiers. Further optimization of this region would be beneficial in terms of operating at the lowest possible channel-stop potential. In order to accommodate the relatively high channel-stop potentials, *e.g.* ≈ 70V in the worst case for Fig. 8, we have incorporated power-semiconductor techniques in these CCDs to reduce electric fields at the termination of the p$^+$ guard rings that are placed close to the output transistors and elsewhere.

3.3. Dark current considerations for overdepleted operation

There is one other significant issue for high-voltage operation of fully depleted CCDs. In overdepletion the electric field at the backside n$^+$ ohmic contact is[6]

$$E_{\text{back}} \equiv -\frac{dV}{dy}(y_J + y_N) = -\left(\frac{V_{\text{sub}} - V_J}{y_N} - \frac{\rho_n}{\epsilon_{\text{Si}}} y_N \right) \tag{5}$$

where ρ_n is $q\, N_{D,\text{sub}}$. This field can be several thousand V/cm at the backside n$^+$ ohmic contact under the conditions typical for the CCDs considered in this work. This high field places stringent demands on the quality of the backside n$^+$ ohmic contact, which must be thin for good blue response but also must be capable of withstanding these high electric fields without an increase in dark current. We use in-situ doped (phosphorus) polysilicon for the backside n$^+$ ohmic contact.[5,6]

Figure 9 shows sub-images taken on a 10.5 μm pixel CCD at -140 °C at substrate bias voltages of 160, 180, and 200V. The sub-image is approximately 290 $\times$ 220 pixels, and the readout direction is towards the
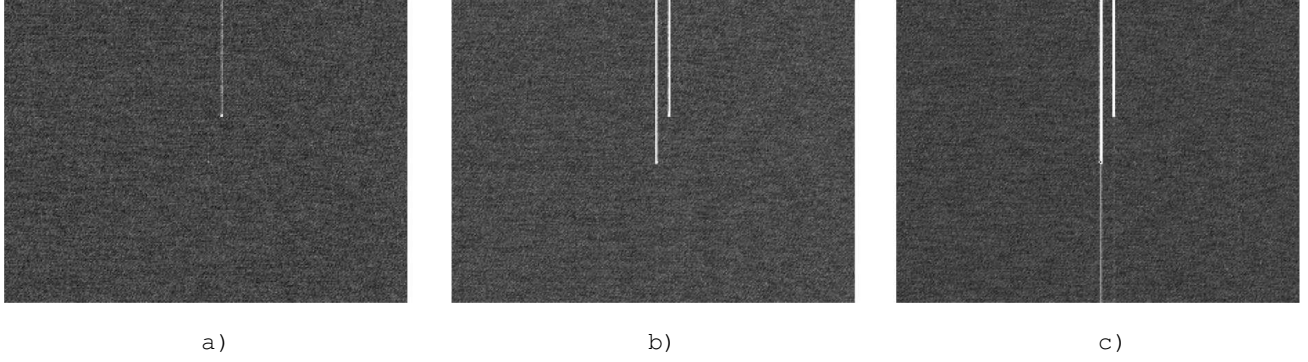
Figure 9. Sub-images of a 10.5 μm pixel CCD taken under dark conditions at -140 °C for various substrate bias voltages. The readout direction is to the bottom. The images were taken by immediately reading out the CCD after a clear operation. The readout time is approximately 12 seconds. The sub-images are approximately 290 $\times$ 220 pixels. a) 160V, b) 180V, and c) 200V.
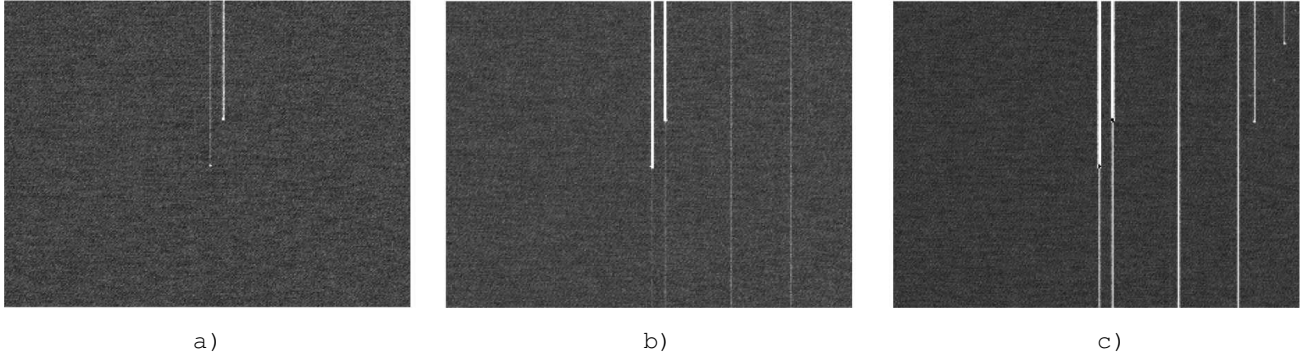

Figure 10. Sub-images of a 10.5 μm pixel CCD taken under dark conditions at 170V substrate bias for various operating temperatures. The readout direction is to the bottom. The images were taken by immediately reading out the CCD after a clear operation. The readout time is approximately 12 seconds. The sub-images are approximately 290 $\times$ 220 pixels, and the sub-image area is the same as in Fig. 9. a) -140 °C, b) -120 °C, and c) -105 °C.

bottom of the images. At 160V a hot pixel is observed, and this hot pixel injects charge during the readout leading to the excess charge observed above the hot pixel location. At 180V the charge injected at the hot pixel has increased by about a factor of five, and another hot pixel is observed to the left of the original hot pixel. Increasing the substrate bias voltage to 200V results in another increase of nearly five in the charge injected at both hot pixels. This exponentially increasing current with substrate bias voltage has also been observed at room temperature in a low percentage of photodiodes fabricated with a similar process to that used for CCD fabrication. In the photodiode case we see an exponentially increasing dark current at substrate bias voltages approximately corresponding to full depletion. We believe the hot pixels shown in Fig. 9 are of the same origin, and arise from defects at or near the backside n$^+$ ohmic contact.

Figure 10 shows the temperature dependence of hot pixels for the same sub-image area of Fig. 9. In this case the substrate bias voltage is held constant at 170V, and the temperature is increased from -140 °C to -120 °C and then to -105 °C. A strong temperature dependence is observed, and new defects are seen as the temperature is raised. We believe the strong dependence on temperature and substrate bias voltage of the dark current from the backside defects is an indication of a trap-assisted tunneling phenomena perhaps including Frenkel-Poole barrier lowering.[18–20] In trap-assisted tunneling the strong temperature dependence comes from the thermal excitation of carriers to the trap level. Once a trap is filled, the electron can quantum mechanically tunnel to the conduction band with an exponential dependence on the local electric field.
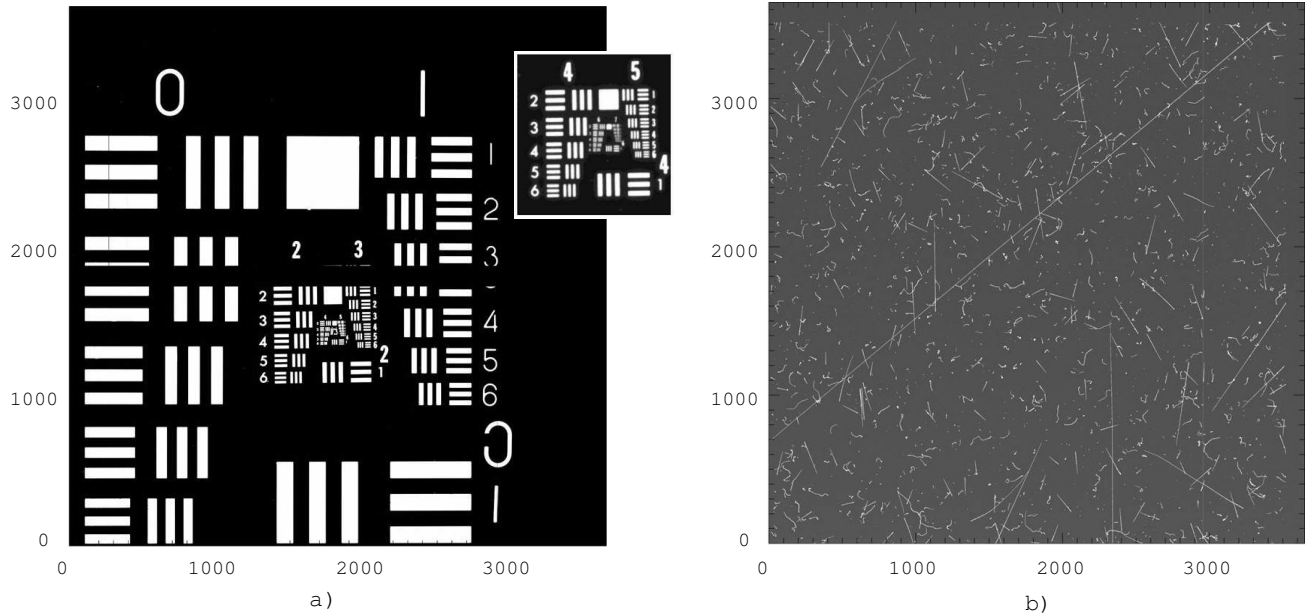
Figure 11. Images taken on a 3512×3512, 10.5 μm pixel CCDs at 200V substrate bias. a) Test pattern taken on 200 μm thick, back-illuminated CCD 105868-13-6 at -140 °C. The inset is a magnified view of the test patterns with the smallest feature sizes. b) 30 minute dark current image taken on ≈ 650 μm thick, front-illuminated CCD 107409-16-11. The measured dark current at -140 °C was 0.63 electrons/pixel-hour. The trails are cosmic rays and Compton electrons from natural background radiation.

4. HIGH-VOLTAGE-COMPATIBLE CCD RESULTS

Two lots of 3512^2, 10.5 μm pixel CCDs were fabricated at DALSA Semiconductor, and in each lot a small number of 650–675 μm-thick wafers were completely finished for process monitoring and quality control purposes. In addition, a larger number of wafers were partially fabricated at DALSA Semiconductor with the processing necessary to produce back-illuminated CCDs done at LBNL.[7] The field-oxide thickness in one of the lots was ≈ 0.5 μm, and in the other lot a processing split was done to produce field-oxide thicknesses of ≈ 0.5 and 0.25 μm.

Figure 11 shows measured results on CCDs from these lots that were operated at 200V substrate bias, which is the limit of our test setup. Figure 11 a) shows a test pattern image taken on a 200 μm thick, back-illuminated CCD. This was the first large format, 200 μm thick CCD produced in our laboratory that functioned at such a high substrate bias voltage with no deleterious effects. Although we have no immediate plans for 200V-compatible, 200 μm-thick CCDs, the ability to operate at such high voltages is an important milestone towards the goal of space qualification of fully depleted CCDs that will be used at substrate bias voltages in the 80–110V range. As described earlier, this range of substrate bias voltage is necessary in order to meet the PSF requirements for SNAP.

The ability to operate at high substrate bias voltages improves the PSF for a given thickness (Fig. 1), but also allows for full depletion of thicker CCDs. From simple p-n junction theory the voltage necessary for full depletion goes as the square of thickness, and therefore high-voltage operation is required to deplete thick devices. Figure 11 b) shows cosmic rays and background radiation events[21] observed after a 30 minute integration in the dark for a fully depleted, ≈ 650 μm thick, front-illuminated CCD operated at -140 °C. This CCD was completely fabricated at DALSA Semiconductor. The measured dark current was 0.63 electrons/pixel-hour. Full depletion was verified by the lack of spatial blooming on the tails of the cosmic ray and radiation events, which were pronounced on this and other CCDs operated partially depleted.

Fully depleted, thick CCDs can have applications in the direct detection of x rays. A 200 μm thick CCD is nearly 100% efficient for the detection of 8 keV x rays, and a 650 μm thick CCD has approximately 50% efficiency for 20 keV x rays.[22] Figure 12 shows direct x-ray imaging results with a 3512^2, 10.5 μm, 200 μm
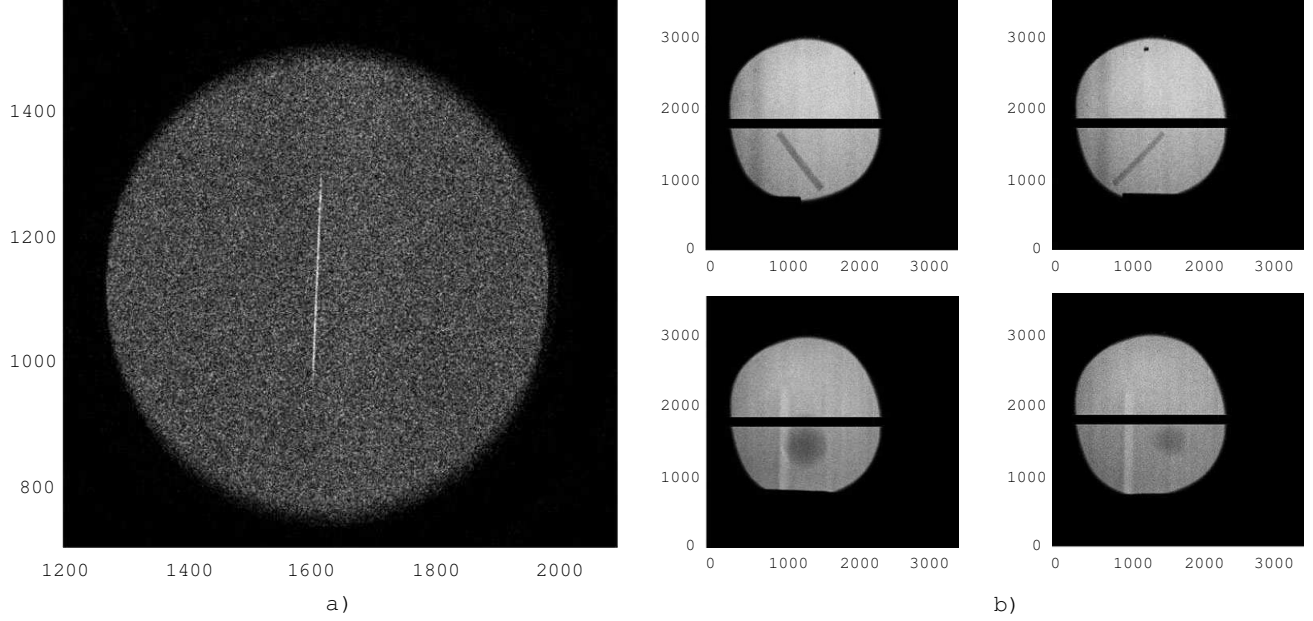
Figure 12. Demonstration of the direct detection of x rays with thick, fully depleted CCDs. In all cases the circular aperture is defined by a Be entry window with good x-ray transmission. All measurements were done at -140 °C. The CCD format was 3512^2 with 10.5 μm pixels, and the CCD was 200 μm thick. A Ni K-edge filter was used to attenuate the higher-energy bremsstrahlung from the Cu anode x-ray source that was operated at 15 keV and 5 mA. a) x-ray transmission image of a stainless-steel target with a 5 μm slit. b) Imaging at 8 keV of an x-ray phantom. The upper images are of nylon fibers, and the lower images are simulated tumor-like masses. The speck in the upper right image is a simulated micro-calcification.

thick CCD operated in a cryogenic dewar with a Be window used to allow for good transmission of x rays to the CCD. The x rays were provided by a Cu anode x-ray tube operating at 15 keV. A Ni K-edge filter was used to attenuate the higher-energy bremsstrahlung x rays, yielding predominantly 8.04 keV K-α x rays from the Cu anode. Figure 12 a) shows an x-ray transmission image of a stainless-steel target with a 5 μm slit. The target was partially transparent to the 8 keV x rays, but the slit is still easily visible. Figure 12 b) shows imaging done on part of a mammography x-ray phantom.[23] The phantom consists of two parts, a 0.7 cm thick paraffin insert with embedded test objects, and a 3.3 cm thick acrylic base that simulates 4.2 cm of compressed breast tissue. Only the paraffin insert was used for imaging because the acrylic base was strongly absorbing for 8 keV x rays.

There is a photon dynamic range issue with direct x-ray imaging of high-energy x rays since the number of electron-hole pairs produced per x-ray photon is $E_{\mathrm{photon}}/3.65$, where E_{photon} is the photon energy in eV. At high x-ray energies the CCD full well limits the x-ray-photon dynamic range, and broadband x-ray sources further contribute to contrast difficulties when directly imaging high-energy x rays. These problems can be reduced with future developments in high-speed readout that will allow frame-by-frame summation to increase the dynamic range.

5. CONCLUSIONS

We have described the motivation for and issues related to the development of high-voltage-compatible, fully depleted CCDs fabricated on high-resistivity, n-type silicon. Experimental results showing 200 μm-thick CCD operation at substrate bias voltages of 200V have been described, as well as the demonstration of full depletion of 650 μm thick CCDs. In addition to the planned application of low-light level detection for these CCDs, we have discussed and demonstrated direct detection of 8 keV x rays with nearly 100% detection efficiency.

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REFERENCES

1. J.C. Geary, "The LSST sensor technologies studies," this Proceedings.
2. B. Flaugher, "The dark energy survey," *Inter. J. of Modern Phys. A*, **20**, pp. 3121–3123, 2005.
3. Y. Kamata *et al.*, "Development of thick back-illuminated CCD to improve quantum efficiency in optical longer wavelength using high-resistivity n-type silicon," *Proc. of SPIE*, **5499**, pp. 210–218, 2004.
4. G. Aldering *et al.*, "Overview of the Supernova/Acceleration Probe (SNAP)," *Proc. of SPIE*, **4835**, pp. 146–157, 2002.
5. S.E. Holland *et al.*, "A 200 × 200 CCD image sensor fabricated on high-resistivity silicon," in *IEDM Technical Digest*, pp. 911–914, 1996.
6. S.E. Holland, D.E. Groom, N.P. Palaio, R.J. Stover, and M. Wei, "Fully depleted, back-illuminated charge-coupled devices fabricated on high-resistivity silicon," *IEEE Trans. Elec. Dev.*, **50**, pp. 225–238, 2003.
7. C. J. Bebek *et al.*, "Development of fully depleted, back-illuminated charge coupled devices," *Proc. of SPIE*, **5499**, pp. 140–150, 2004.
8. C. J. Bebek *et al.*, "Fully depleted back-illuminated p-channel CCD development," *Proc. of SPIE*, **5167**, pp. 60–62, 2003.
9. Y. Bai *et al.*, "Hybrid CMOS focal plane array with extended UV and NIR response for space applications," *Proc. of SPIE*, **5167**, pp. 83–93, 2004.
10. A.W. Hoffman, P.J. Love, K.J. Ando, and E. Corrales, "Large infrared and visible arrays for low-background applications: an overview of current developments at Raytheon," *Proc. of SPIE*, **5499**, pp. 240–249, 2004.
11. J.A. Fairfield *et al.*, "Improved spatial resolution in thick, fully depleted CCDs with enhanced red sensitivity," *IEEE Trans. Nucl. Sci.*, submitted for publication.
12. J.R. Janesick, *Scientific charge-coupled devices*, pp. 618–621, SPIE Press, Bellingham, WA, 2001.
13. J.-I. Nishizawa, T. Terasaki, and J. Shibata, "Field-effect transistor versus analog transistor (static induction transistor)," *IEEE Trans. Elec. Dev.*, **22**, pp. 186–197, 1975.
14. B.E. Burke *et al.*, "CCD soft-x-ray detectors with improved high- and low-energy performance," *IEEE Trans. Nucl. Sci.*, **51**, pp. 2322–2327, 2004.
15. TSUPREM4 Version X-2005.10-0 and Medici Version W-2004.09-0, Synopsis, Inc., Mountain View, CA.
16. B.E. Burke and S.A. Gajar, "Dynamic suppression of interface-state dark current in buried-channel CCDs," *IEEE Trans. Elec. Dev.*, **38**, pp. 285–290, February 1991.
17. R.H. Richter *et al.*, "Strip detector design for ATLAS and HERA-B using two-dimensional device simulation," *Nucl. Instr. Meth. A*, **377**, pp. 412–421, 1996.
18. G. Vincent, A. Chantre, and D. Bois, "Electric field effect on the thermal emission of traps in semiconductor junctions," *J. Appl. Phys.*, **50**, pp. 5484–5487, 1979.
19. A. Schenk, "A model for the field and temperature dependence of Shockley-Read-Hall lifetimes in silicon," *Solid-State Elec.*, **35**, pp. 1585–1596, 1992.
20. M. Tsuchiaki, H. Fujimori, T. Iinuma, and A. Kawasaki, "An interface state mediated junction leakage mechanism induced by a single polyhedral oxide precipitate in silicon diode," *J. Appl. Phys.*, **85**, pp. 8255–8266, 1999.
21. A. R. Smith *et al.*, "Radiation events in astronomical CCD images," *Proc. of SPIE*, **4669**, pp. 172–183, 2002.
22. National Institutes of Standards Physical Reference Data, http://www.physics.nist.gov/PhysRefData/XrayMassCoef/cover.html.
23. Mammography x-ray phantom, Gammex RMI, Middleton, WI.